Claim Amendments

Please amend claims 1, 3, 7, 9, 14, 17, 19, and 23 as follows:

Claims as Amended

What is claimed is:

1. (currently amended) A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in a polysilicon gate electrode etching process comprising the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

~~patterning the hardmask layer for forming a gate electrode according to a photolithographic patterning process~~;

carrying out a first reactive[[on]] ion etch (RIE) step to etch through a thickness of the hardmask layer to expose the polysilicon layer to form a patterned hard mask for forming a gate electrode;

carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power;

carrying out a third RIE step to etch through a second thickness portion of the polysilicon layer to expose portions of an underlying gate dielectric including ~~at least one of~~ using lower etch power compared to the second RIE step, said lower power selected from the group consisting of a lower RF source power and a lower RF bias power ~~compared to the second RIE step~~; and,

plasma treating the exposed gate dielectric and polysilicon layer in-situ wherein the plasma is formed essentially from an inert source gas to neutralize an electrical charge imbalance ~~; and,~~

~~carrying out a fourth RIE etch process to etch through a remaining thickness of the polysilicon layer.~~

2. (original) The method of claim 1, wherein the step of plasma treating is carried out using zero RF bias power.

3. (currently amended) The method of claim 1, ~~wherein the fourth~~ further comprising an RIE overetch ~~process is~~ step carried out using zero RF bias power.

4. (original) The method of claim 1, wherein the polysilicon layer includes an n-dope region and a p-doped region for forming respectively doped polysilicon gate electrodes in parallel.

5. (original) The method of claim 1, wherein the RF source power and RF bias power are reduced in the third RIE Step.

6. (original) The method of claim 1, wherein the inert gas source is selected from the group consisting of argon, helium, nitrogen, and mixtures thereof.

7. (currently amended) The method of claim 1, wherein ~~the fourth~~ further comprising an RIE overetch [[is]] step carried out with a chlorine-free etching chemistry.

8. (original) The method of claim 7, wherein the chlorine-free etching chemistry comprises HBr and oxygen.

9. (currently amended) The method of claim 1, wherein the second

and third RIE etch steps have an etching chemistry comprising constituents selected from the group consisting of ~~the combination of one of~~ $HBr/Cl_2/O_2$ and $CF_4/Cl_2/O_2$.

10. (original) The method of claim 1, wherein the RF bias power is supplied at a frequency of greater than about 1 MHz adjustably decoupled from the RF source power.

11. (original) The method of claim 1, wherein the gate dielectric is selected from the group consisting of thermally grown SiO_2 and binary oxides having a dielectric constant of greater than about 20.

12. (original) The method of claim 1, wherein the hardmask layer is selected from the group consisting of silicon oxide, silicon nitride, and silicon oxynitride.

13. (original) The method of claim 1, wherein the third RIE etch step is carried out with zero RF bias power applied.

14. (currently amended) A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching in parallel etching of n and p-doped polysilicon gate electrodes comprising

the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer including n-doped and p-doped regions formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

~~patterning the hardmask layer according to a photolithographic patterning process for forming a polysilicon gate electrode;~~

carrying out a first reaction ion etch (RIE) step to etch through a thickness of the hardmask layer to expose portions of the polysilicon layer to thereby form a patterned hard mask for forming gate electrode;

carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power.

carrying out a third RIE step to etch through a second

thickness portion of the polysilicon layer to expose portions of an underlying gate dielectric ~~including at least one of~~ using lower etch power compared to the second RIE step, said lower power selected from the group consisting of a lower RF source power and a lower RF bias power ~~compared to the second RIE step to expose a portion of the gate dielectric;~~

then plasma treating in-situ with an inert gas plasma the exposed gate dielectric and polysilicon layer using a zero RF bias power to neutralize an electrical charge imbalance ~~on the polysilicon gate electrode~~; and,

then carrying out an ~~fourth~~ RIE overetch process to etch ~~through~~ remove a remaining ~~thickness~~ portions of the polysilicon layer using a zero RF bias power.

15. (original) The method of claim 14, wherein the RF source power and RF bias power are reduced in the third RIE Step.

16. (original) The method of claim 14, wherein the inert gas source is selected from the group consisting of argon, helium, nitrogen, and mixtures thereof.

17. (currently amended) The method of claim 14, wherein the fourth RIE overetch is carried out with a chlorine-free etching chemistry.

18. (original) The method of claim 17, wherein the chlorine-free etching chemistry comprises HBr and oxygen.

19. (currently amended) The method of claim 14, wherein the second and third RIE etch steps have an etching chemistry selected from the group consisting of HBr, Cl_2, CF_4, and O_2 ~~comprising the combination of one of HBr/Cl_2/O_2 and CF_4/Cl_2/O_2~~.

20. (original) The method of claim 14, wherein the RF bias power is supplied at a frequency of greater than about 1 MHz adjustably decoupled from the RF source power.

21. (original) The method of claim 14, wherein the gate dielectric is selected from the group consisting of thermally grown SiO_2 and binary lanthanum oxides having a dielectric constant of greater than about 20.

22. (original) The method of claim 14, wherein the hardmask layer is selected from the group consisting of silicon oxide, silicon

nitride, and silicon oxynitride.

23. (currently amended) The method of claim 14, wherein the ~~second~~ third RIE etch step is carried out with zero RF bias power applied.